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Department of Electronics and Communication Engineering

For the academic year 2021-22, the students of Electronics and Communication Engineering have undergone Mini Projects with Hardware Development as well as software implementation in their M.Tech as prescribed by JNTUH, Hyderabad in the Curriculum.

S.No	Description	No. of Students	Page No.	
1	Mini Projects	8	2-10	
	Total Number of Students:	8		

PRINCIPAL

Vignan's lastitute of Management & Technology For Women Kondessa (V) And area (M) Madeiral Matkajgiri (Dt) - 50 % %

Telengana State



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Kondapur (V), Ghatkesar (M), Medchal - Malkajgiri (D) - 501 301 Phone: +91 96529 10002/3



Department of Electronics and Communication Engineering

Admitted Batch: 2021

A.Y. 2021-2022

M.TECH-II SEM- MINI PROJECT LIST

S.No	Batch No	Roll Number	Student Name	Title Name	Guide Name
1	A1	21UP1D5703	K.AKSHITHA	Design and Simulation of Low Power Wilson Current Mirror And Single Supply Cmos Level Shifter	Dr. SK. Masthan Basha
2	A2	21UP1D5702	KASARAGADDA PRAVALLIKA	Implementation of Low Power 1-bit Hybrid Full Adder using 16nm CMOS Technology	Mr.E.Nagaraju
3	A3	21UP1D5704	K. ANITHA DEVI	High-Speed Hybrid-Logic Full Adder Using High- Performance 10-T Xor- Xnor Cell	Mr. T Pullaish
4	A4	21UP1D5706	S. MANIDEEPA	The three stage comparator and its modified version with fast speed and low kick back	Dr. SK. Masthan Basha
5	A5	21UP1D5707	A. JHANSI RANI	Design and Implementation of low power high performance mixed logic line Decoders	Mrs. S Shilpa
6	A6	21UP1D5705	PUNEM SANGEETHA	Study Of Different Adders Usingfull Swing Gate Diffusion Input	Dr. Vijaykumar R Urkude
7	A7	21UP1D5708	MAHARAJA SANGEETHA	Area Optimization Of Cmos Full Adder Design Using 3txor	Mrs. G Swathi
8	A8	21UP1D5701	B.USHA	Relpee: Resistive RAM- sedlinear first order partial differential equationsolver	Mrs. G Susmitha

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "DESING AND SIMULATION OF LOW POWER WILSON CURRENT MIRROR AND SINGLE SUPPLY CMOS LEVEL SHIFTER" Submitted by Miss KAKSHITHA (RegdNo.21UP1D5703) in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

The results embodied in this mini project report have not been submitted in any University for the award of any degree and the results are achieved satisfactorily.

Mr. P Hari Krishna

Dr.SK Masthan Basha

AssociateProfessor

Head of the Department

Head of the Department Jectronics and Communication Engineering Fignan's Institute of Management and Technology for Women Kondapur (V), Ghalkesar (M), R.R. Dist-501 301

Visnan's Institute of Management & Technology For Women Kondapur(V), Ghatkesar(M), Medchal-Malkajgiri(Dt)-501301 Telangana State

VIGNAN'S INSTITUTE OF MANAGEMENT AND TECHNOLOGY FOR WOMEN DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled IMPLEMENTATION OF LOW POWER1-BIT HYBRID FULL ADDER USING 16 NM CMOS TECHNOLOGY" submitted by Ms. Kasaragadda Pravallika (RegdNo.21UP1D5702) in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSIDESIGN to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Mr. P. HariKrishna

Mr.E.NAGARAJU

Head of the Department
Head of the Department
Electronics and Communication Engineering
Vignon's Institute of Management and Technology for Women
Kondapur (V), Ghatkesar (M), R.R. Dist-501 301

AssistantProfessor

PRINCIPAL

"Innea's Institute of Management & Technology For Women
Action (V), Ghetkesar(M), Medchel-Malkejgiri (Dt)-501301

Telangane State

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "HIGH-SPEED HYBRID-LOGIC FULL ADDER USING HIGH-PERFORMANCE 10-T XOR-XNOR CELL" submitted by Ms K.ANITHADEVI(Regd No. 21UP1D5704) in partial fulfilment of the requirements for the award of the degree of Master of Technology in VLSI DESIGN to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Mr.P Hari Krishna

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Kondepur (V), Otastress: (M), Medchel Malkelgiri (OL.) Pin-501301 (T.S.) Associate Professor

PRINCIPAL

Vignan's Institute of Management & Technology For Woman

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Kondepuny Astronom (A) Asocchal-Mukajsin(D4)-501301

Telangens State

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi. Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "THE THREE-STAGE COMPARATOR AND ITS MODIFIED VERSION WITH FAST SPEED AND LOW KICKBACK" submitted by Ms S.Manideepa (Regd No. 21UP1D5706) in partial fulfilment of the requirements for the award of the degree of Master of Technology in VLSI DESIGN to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Mr. P Hari Krishna

Dr. Shaik Masthan Basha

Head of the Department

Head of the Department Flectronics and Communication Engineering Vignan's Institute of Monagement and Technology for Women Kondapur (V), Ghatkesar (M), R.R. Dist-501 301

Associate Professor

Vienan's Institute of Management & Technology For Women Kandapur(V), Ghaikeser(M), Medchel-Malkejgiri(Dt)-501301 Telangana State

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal -- Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "DESIGN AND IMPLEMENTATION OF LOW POWER HIGH PERFORMANCE MIXED LOGIC LINE DECODERS" Submitted by A.Jhansi Rani (RegdNo.21UP1D5707) in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Mr. P Hari Krishna

Head of the Training with iestrHead of the Department Louis Institute of Monaga, and had before legy for Monate

riondapur (V), Ghatkasat (M), R.R. Dist-601 301

Mrs. S Shilpa

Assistant Professor

PRINCIPAL Vignan's Institute of Management & Technology For Women Kondepur(V], @holimasir(VI), Medchal-Malkelgiri(Dt)-501301 Telengana State

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "STUDY OF DIFFERENT ADDERS USINGFULL SWING GATE DIFFUSION INPUT" Submitted by Punem Sangeetha (RegdNo.21UP1D5705) in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Mr. P Hari Krishna

Dr. Vijay Kumar R Urkude

Head of the Department

Head of the Department Tectronics and Communication Engineering ignon's Institute of Annuages and Ltd Technology for Women Kondapur (V), Ghatkesar (M), R.R. Dist-501 301

AssociateProfessor

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Pin-601301
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "AREA OPTIMIZATION OF CMOS FULL ADDER DESIGN USING 3TXOR" Submitted by Maharaja Sangeetha (RegdNo.21UP1D5708) in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Mr. P'Hari Krishna

Head of the Department

Pleatronies a. A Common extent Engineering -unen's Institute of All magistress and Technology for Women condapur (V), Gharkesar (M), R.R. Dist-501 301

Mrs. G Swathi

Assistant Professor

PRINCIPAL

Vignac's Institute of Management & Tachnelogy For Women Kondapur(V), Chadhasar(M), Madchal-Maikelgiri(Dt)-501301

Telengone State

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Approved By AICTE, New Delhi, Affiliated to JNTUH, Hyderabad) Kondapur (V), Ghatkesar (M), Medchal – Malkajgiri Dist-501301

2021-22



CERTIFICATE

This is to certify that the thesis work titled "RELOPE:RESISTIVE RAM-SEDLINEAR FIRST-ORDER PARTIAL DIFFERENTIAL EQUATIONS OLVER" submitted by Ms B.USHA (Regd No. 21UP1D5701) in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI DESIGN to the Vignan's Institute of Management and Technology for Women, Ghatkesar is a record of bonafide work carried out by her under my guidance and supervision.

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Head of the Department Meetronies and Communication Engineering Vigitan's Institute of Management and Fechnology for Women Kondabur (V), Ghatkesar (M), R.R. Dist-501 301

Assistar Professor

Youth's Institute of Management & Technology For Wome. helifabur(V), Ghalkesar(M), Medchel-Malkajgiri(D1)-501301

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